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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/531,287	04/14/2005	Tadaaki Tanimoto	TAM-103	4868

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MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 DIAGONAL ROAD
SUITE 370
ALEXANDRIA, VA 22314

EXAMINER	
PARIHAR, SUCHIN	
ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
06/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/531,287	TANIMOTO ET AL.	
	Examiner	Art Unit	
	Suchin Parihar	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/5/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/531,287, amendment filed 3/21/2007. Claims 1-3 are currently amended. Claims 6-20 are cancelled. Claims 1-5 are currently pending in this application.

2. Applicant's arguments filed 3/21/2007 have been fully considered but they are not persuasive. The applicable prior art rejections from the previous office action are incorporated herein.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1-5 are rejected under 35 U.S.C. 102(e)** as being anticipated by Tojima (US PG Pub 2003/0005392).

5. With respect to claim 1, Tojima teaches a compiler (i.e. build-in C compiler, paragraph [0004]) comprising:

a conversion program (i.e. converting an algorithm C description, paragraph [0012]);

wherein the conversion program can convert first program descriptions (i.e. converting an algorithm C description, paragraph [0012]) described by diverting a

predetermined program language (i.e. C programming language, paragraph [0012]) into circuit descriptions (i.e. converting the functional C description into a RTL level C description, paragraph [0012]);

the first program descriptions contain register assignment statements (i.e. assignment of data to parameters correspond to register parts, paragraph [0092]) with particular operators (i.e. operator such as a multiplier, paragraph [0104]) and clock boundary descriptions (i.e. clock level descriptions, paragraph [0004]), and which permit circuit operations to be specified at a cycle precision (i.e. the execution cycle of each state can be estimated by inserting a clock counting function which enables estimation of processing performance with high precision, paragraph [0017]);

the circuit descriptions specify hardware realizing the circuit operations (i.e. converting an algorithm C language into a functional C description describing control of hardware, paragraph [0012]) specified by the first program descriptions (i.e. RT level C description, paragraph [0012]) in a predetermined hardware description language (RTL, paragraph [0012]) and;

the register assignment statements (see register assignment statements in Figure 11B involving the register "RcrReg") function to allocate a variable of the left-hand side (see variable "TmpCrc" on the left-hand side of the assignment statement "^="" in Figure 11A) to a register (see register address "0x080F" on right-hand side of assignment statement "^=" in Figure 11A), and need one clock (see Figure 4B, Tojima suggests that register assignments take place in one or less clock cycle and otherwise

notes the need for 2 clock cycles as indicated in the comment for "case EXEC" of Figure 4B) for assignment from the right-hand side to the left hand side.

6. With respect to claim 4, Tojima teaches all the elements of claim 1, from which the claim depends. Tojima teaches: wherein the predetermined program language is a C language (i.e. C descriptions, paragraph [0012], also see Fig 1).

7. With respect to claim 5, Tojima teaches all the elements of claim 1, from which the claim depends. Tojima teaches: wherein the hardware description language is a description language of RTL level (i.e. RT level C description, paragraph [0012]).

8. With respect to claim 2, Tojima teaches a compiler (i.e. build-in C compiler, paragraph [0004]) comprising:

a conversion program (i.e. converting an algorithm C description, paragraph [0012]);

wherein the conversion program can convert first program descriptions (i.e. converting an algorithm C description, paragraph [0012]) described by diverting a predetermined program language (i.e. C programming language, paragraph [0012]) can be converted into second program descriptions (i.e. converting into a functional C description, paragraph [0012]) using a predetermined program language (i.e. C programming language, see abstract or paragraph [0012]);

the first program descriptions contain register assignment statements (i.e. assignment of data to parameters correspond to register parts, paragraph [0092]) with particular operators (i.e. operator such as a multiplier, paragraph [0104]) and clock boundary descriptions (i.e. clock level descriptions, paragraph [0004]), and which

permit circuit operations to be specified at a cycle precision (i.e. the execution cycle of each state can be estimated by inserting a clock counting function which enables estimation of processing performance with high precision, paragraph [0017]);

the second program descriptions contain transformed assignment statements into which the register assignment statements are transformed () in order to make states of preceding cycles referable (i.e. returning to the unit of processing A, paragraph [0061]), and register assignment description insertion statements (i.e. inserting a clock description in the functional C description to convert the functional C description into the RT level description, paragraph [0012]) which associate variables of the transformed assignment statements with changes of registers attendant upon cycle changes (i.e. functions are expressed in a language using a register as a variable, in the form of a clock level simulator, paragraph [0003], Examiner notes that this limitation is interpreted as follows: changes in a register leads to a change to its variable), in correspondence with the clock boundary descriptions (i.e. clock level descriptions, paragraph [0004]); and

the register assignment statements (see register assignment statements in Figure 11B involving the register "RcrReg") function to allocate a variable of the left-hand side (see variable "TmpCrc" on the left-hand side of the assignment statement "^="" in Figure 11A) to a register (see register address "0x080F" on right-hand side of assignment statement "^=" in Figure 11A), and need one clock (see Figure 4B, Tojima suggests that register assignments take place in one or less clock cycle and otherwise

notes the need for 2 clock cycles as indicated in the comment for "case EXEC" of Figure 4B) for assignment from the right-hand side to the left hand side.

9. With respect to claim 3, Tojima teaches a compiler (i.e. build-in C compiler, paragraph [0004]) comprising:

a conversion program (i.e. converting an algorithm C description, paragraph [0012]);

wherein the conversion program can convert first program descriptions (i.e. converting an algorithm C description, paragraph [0012]) described by diverting a predetermined program language (i.e. C programming language, paragraph [0012]) into second program descriptions (i.e. converting into a functional C description, paragraph [0012]) using a predetermined program language (i.e. C programming language, see abstract or paragraph [0012]);

the first program descriptions contain register assignment statements (i.e. assignment of data to parameters correspond to register parts, paragraph [0092]) with particular operators (i.e. operator such as a multiplier, paragraph [0104]) and clock boundary descriptions (i.e. clock level descriptions, paragraph [0004]), and which permit circuit operations to be specified at a cycle precision (i.e. the execution cycle of each state can be estimated by inserting a clock counting function which enables estimation of processing performance with high precision, paragraph [0017]);

the second program descriptions contain transformed assignment statements into which the register assignment statements are transformed () in order to make states of preceding cycles referable (i.e. returning to the unit of processing A,

paragraph [0061]), and register assignment description insertion statements (i.e. inserting a clock description in the functional C description to convert the functional C description into the RT level description, paragraph [0012]) which associate variables of the transformed assignment statements with changes of registers attendant upon cycle changes (i.e. functions are expressed in a language using a register as a variable, in the form of a clock level simulator, paragraph [0003], Examiner notes that this limitation is interpreted as follows: changes in a register leads to a change to its variable), in correspondence with the clock boundary descriptions (i.e. clock level descriptions, paragraph [0004]);

the circuit descriptions specify hardware (i.e. a functional C description describing control of hardware, paragraph [0012]) which is defined by the second program descriptions, in a predetermined hardware description language (RTL description, paragraph [0012]); and

the register assignment statements (see register assignment statements in Figure 11B involving the register "RcrReg") function to allocate a variable of the left-hand side (see variable "TmpCrc" on the left-hand side of the assignment statement "^="" in Figure 11A) to a register (see register address "0x080F" on right-hand side of assignment statement "^=" in Figure 11A), and need one clock (see Figure 4B, Tojima suggests that register assignments take place in one or less clock cycle and otherwise notes the need for 2 clock cycles as indicated in the comment for "case EXEC" of Figure 4B) for assignment from the right-hand side to the left hand side.

Response to Arguments

10. Applicant's arguments filed 3/21/2007 have been fully considered but they are not persuasive. Examiner's response to arguments follows below.

11. Applicant asserts that Tojima does not disclose the register assignment statements of the present invention which function to allocate a variable of the left-hand side to a register and need one clock cycle for assignment from the right-hand side to the left-hand side. Examiner disagrees with this assertion.

12. Examiner points out that assignment statements involving assignment between right-hand side and left-hand side using a register and variable are well known in the art, as is suggested by Tojima. With regard to Figure 4B, Tojima discusses the necessity to point out that certain assignment statements require more than one clock cycle, as is indicated by "case EXEC" of figure 4B. It is then implied that the instructions of "case INI" do not require more than one clock cycle. In addition, Figure 11B shows examples of register assignment statements involving the register CrcReg.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suchin Parihar whose telephone number is 571-272-6210. The examiner can normally be reached on Mon-Fri, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Suchin Parihar
Examiner
AU 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER